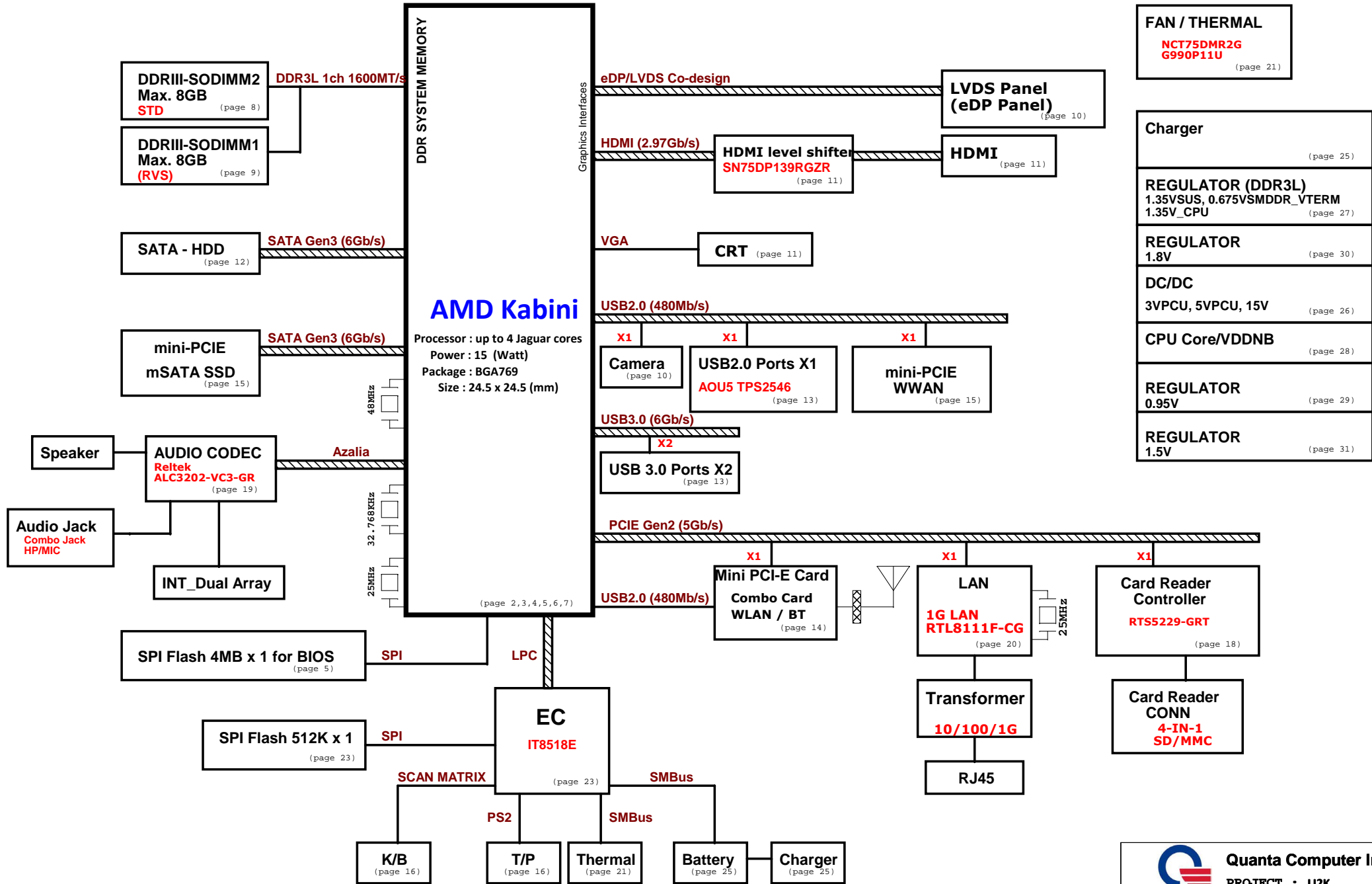






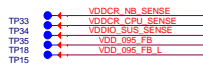
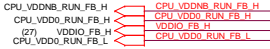
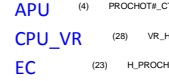
LI2K AMD Kabini Platform UMA Block Diagram





SVC	SVD	Boot Voltage
-----	-----	--------------

	CPU_SVT	(28)
	CPU_SVC	(28)
	CPU_SVD	(28)
	CPU_PWRGD_SVID_REG	(28)



Over Temperature Protection

DEGREE	R476
120	1.74K
110	8.2K
100	15K

(default)

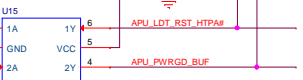
DEGREE	R476
120	1.74K
110	8.2K
100	15K

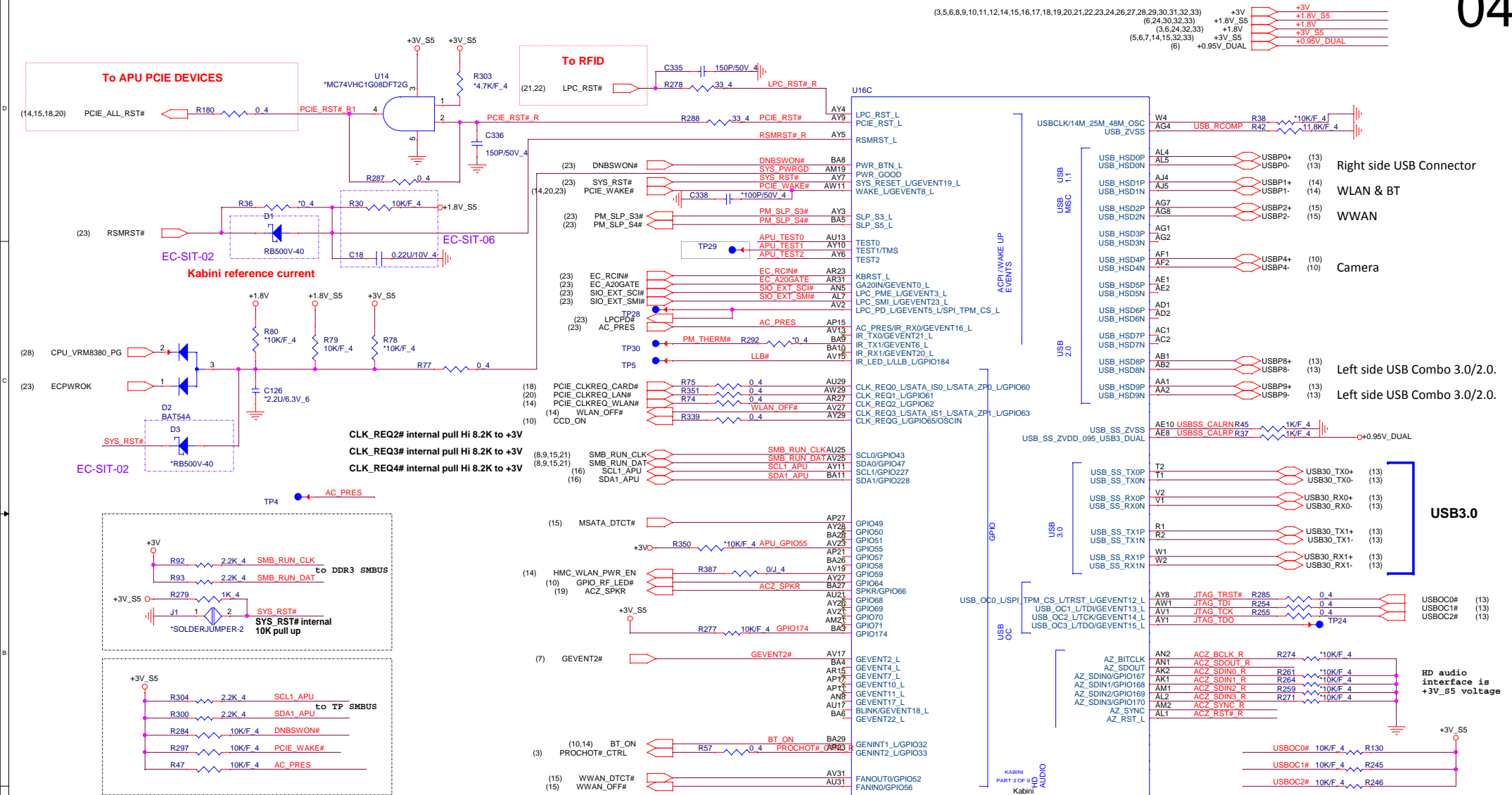
(default)

HDT+ HEADER / PLACE ON TOP

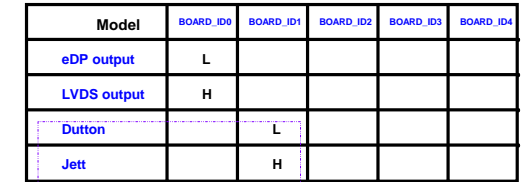


Can remove on MP



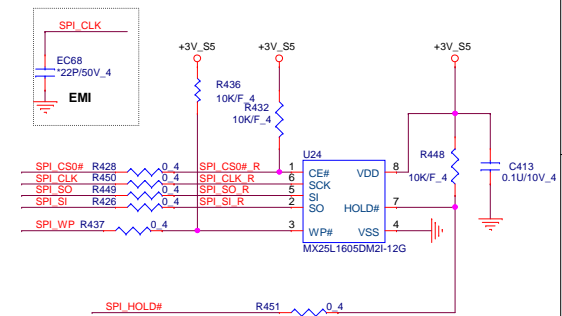


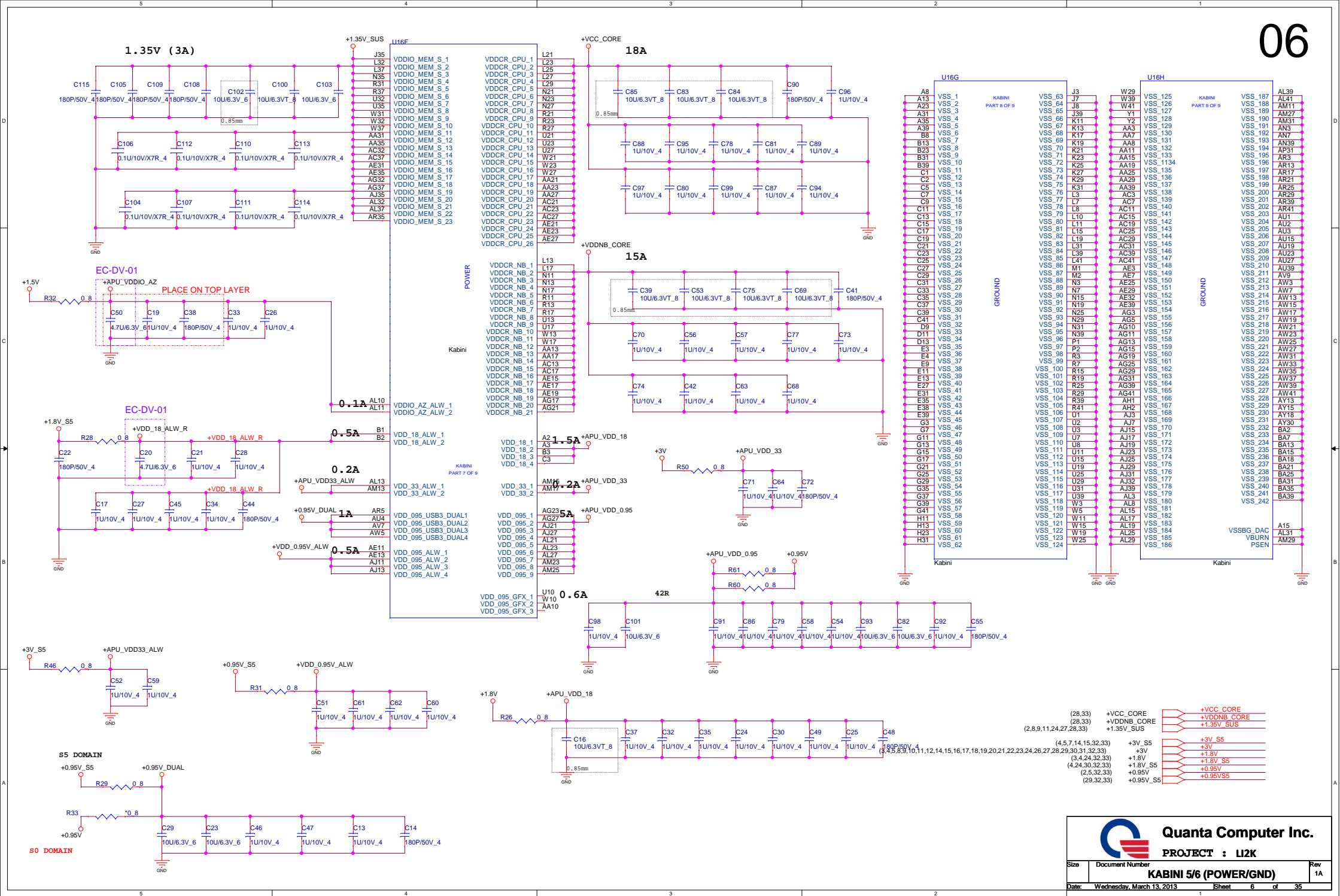
TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



APU SPI ROM
Replace to MX25L6436E

Vender	Size	P/N
EON	4M	AKE39ZN0Q02
WINBOND	4M	AKE391P0N00
Socket		DFHS08FS023

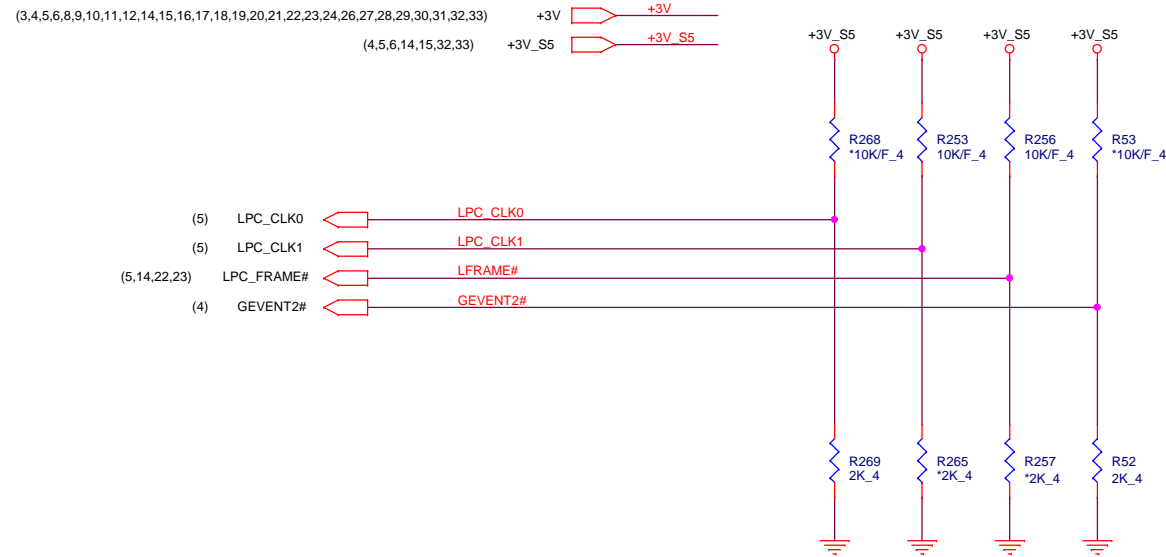






STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

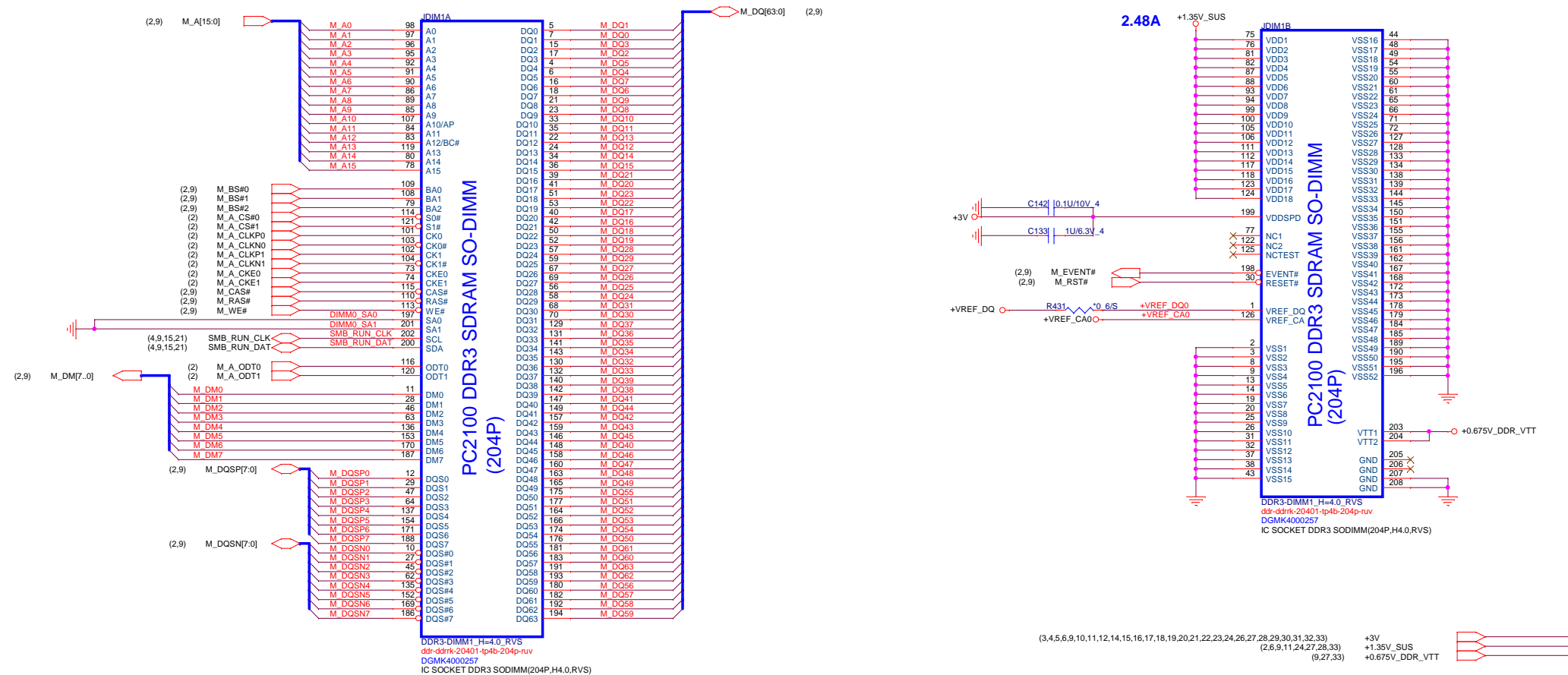
					LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH					BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW					BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

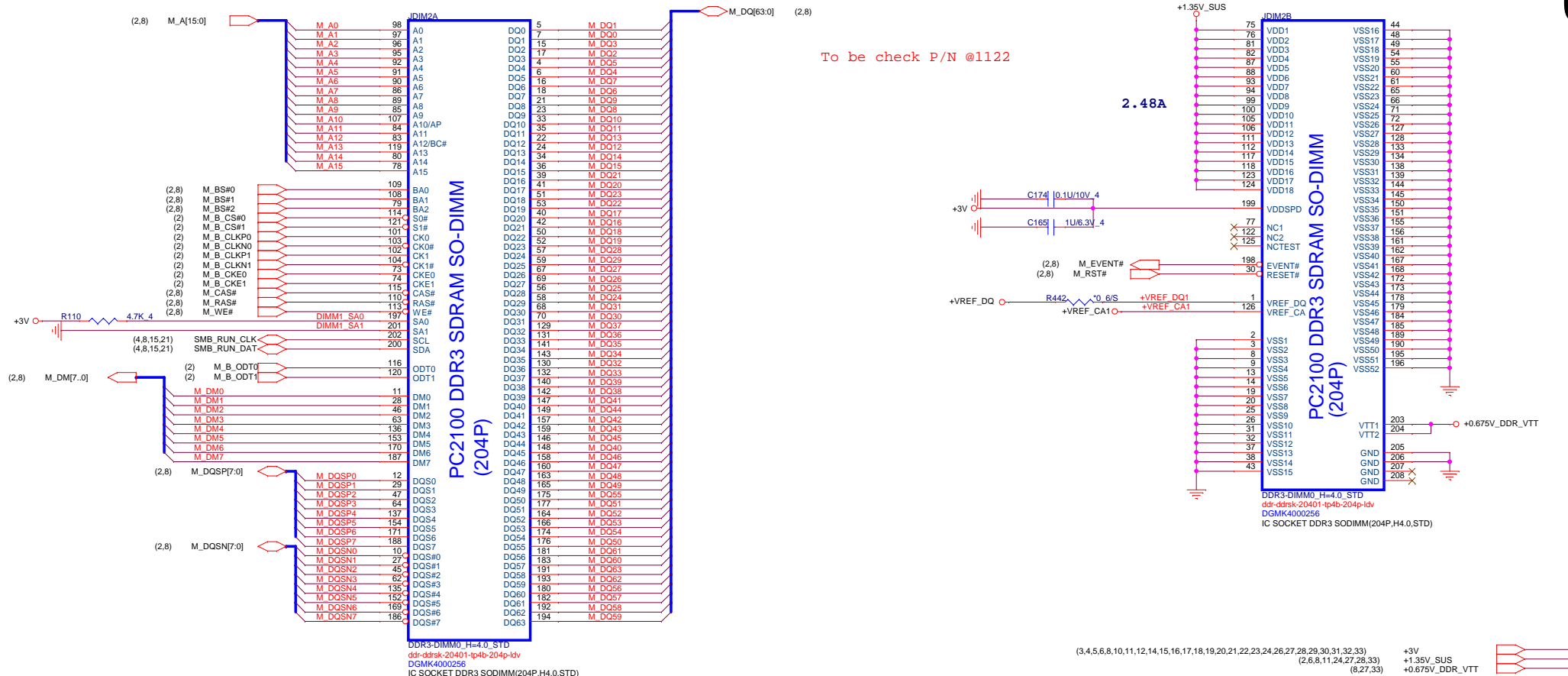


Quanta Computer Inc.

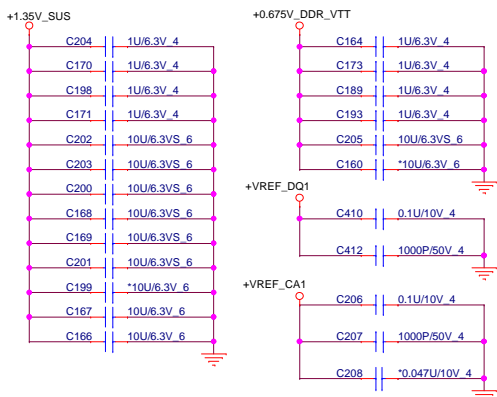
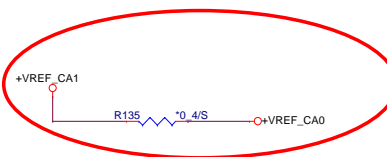
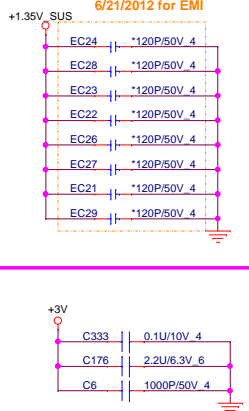
PROJECT : L12K

Size	Document Number	Rev
	KABINI 6/6 (STRAP)	1A
Date:	Wednesday, March 13, 2013	Sheet 7 of 35





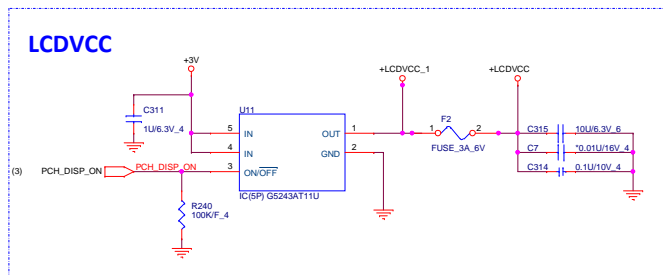
Place these Caps near So-Dimm1.

For EMI RESERVE
6/21/2012 for EMI

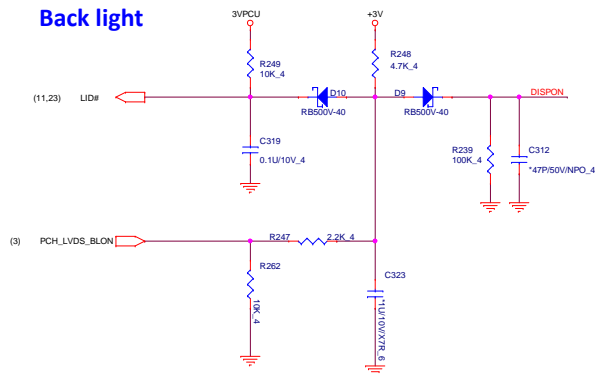
Local Thermal Sensor

Delete the NB5's Thermal Solution @1126 -- ALF

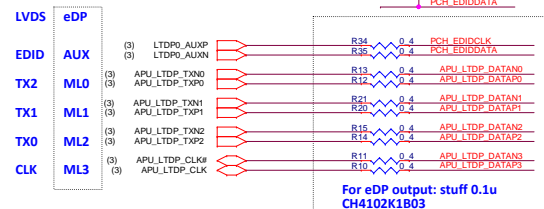
DDR3 Thermal Sensor



Back light

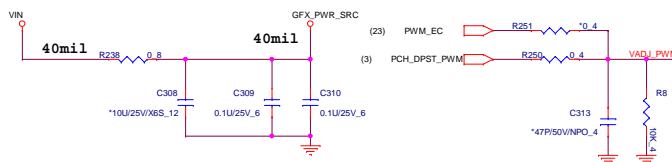


For LVDS only : stuff (default)



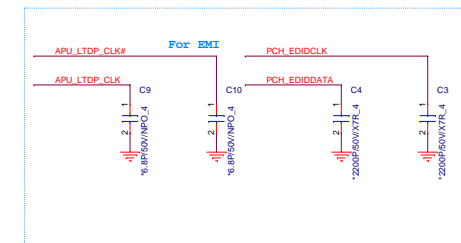
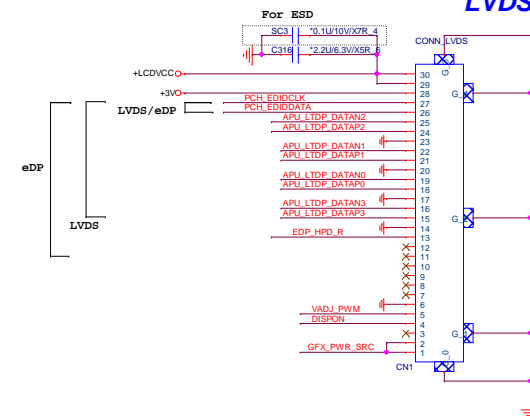
For EDP Only: stuff

GFX_PWR_SRC

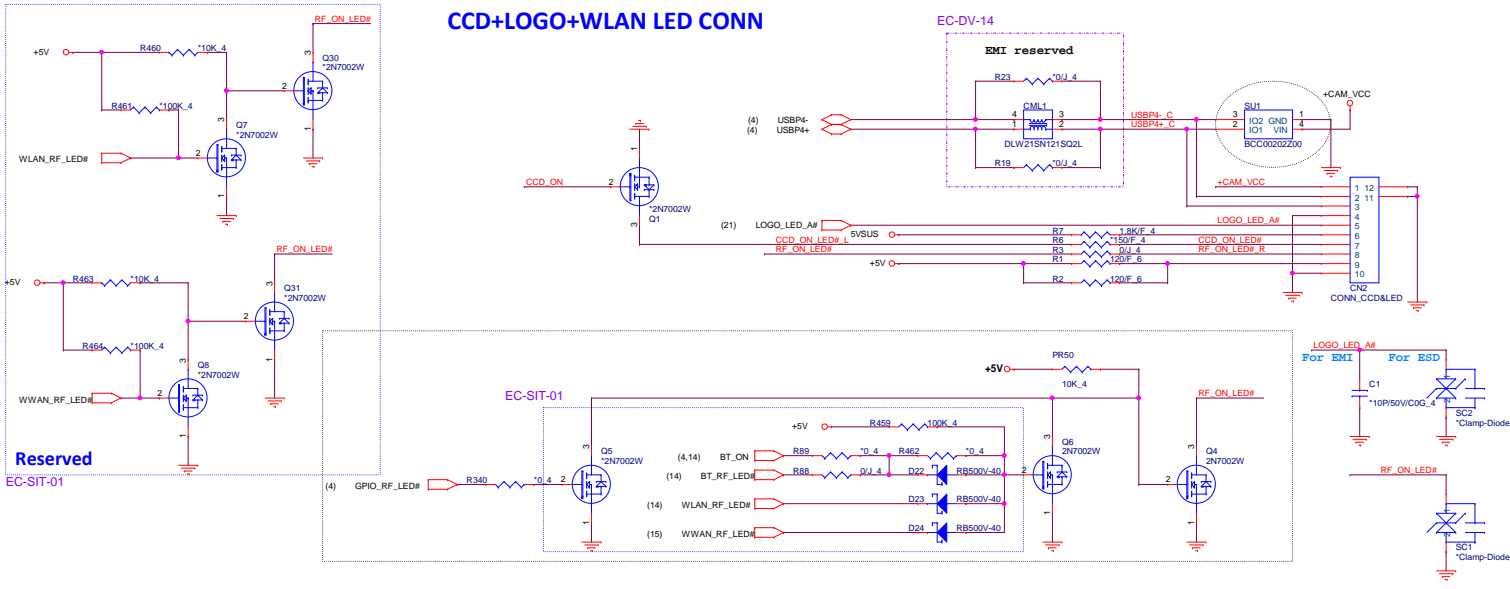


Need to Informa ME have 2 LCD cable,
one is for LVDS, other one is for eDP@1126

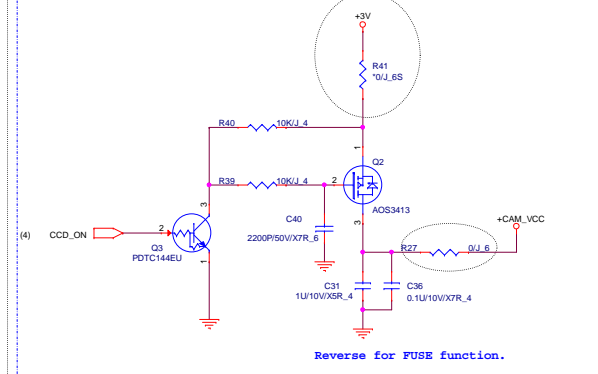
LVDS Conn.



CCD+LOGO+WLAN LED CONN



CAMERA VCC Control

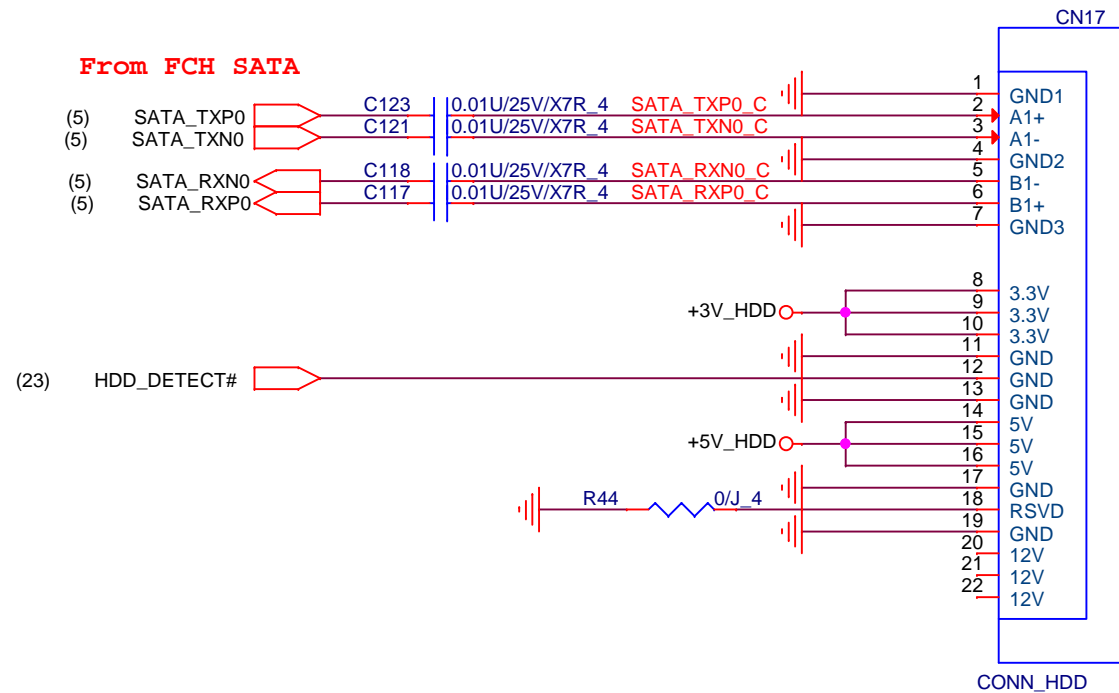


EC-DV-13 EC-SIT-10

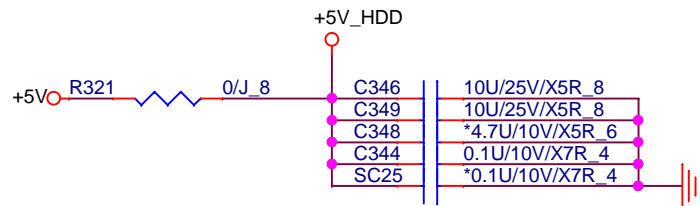


SATA HDD CONN

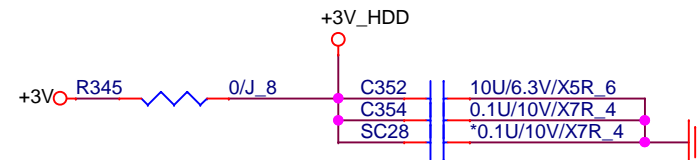
12



DC Current rating: 2 A (MAX)



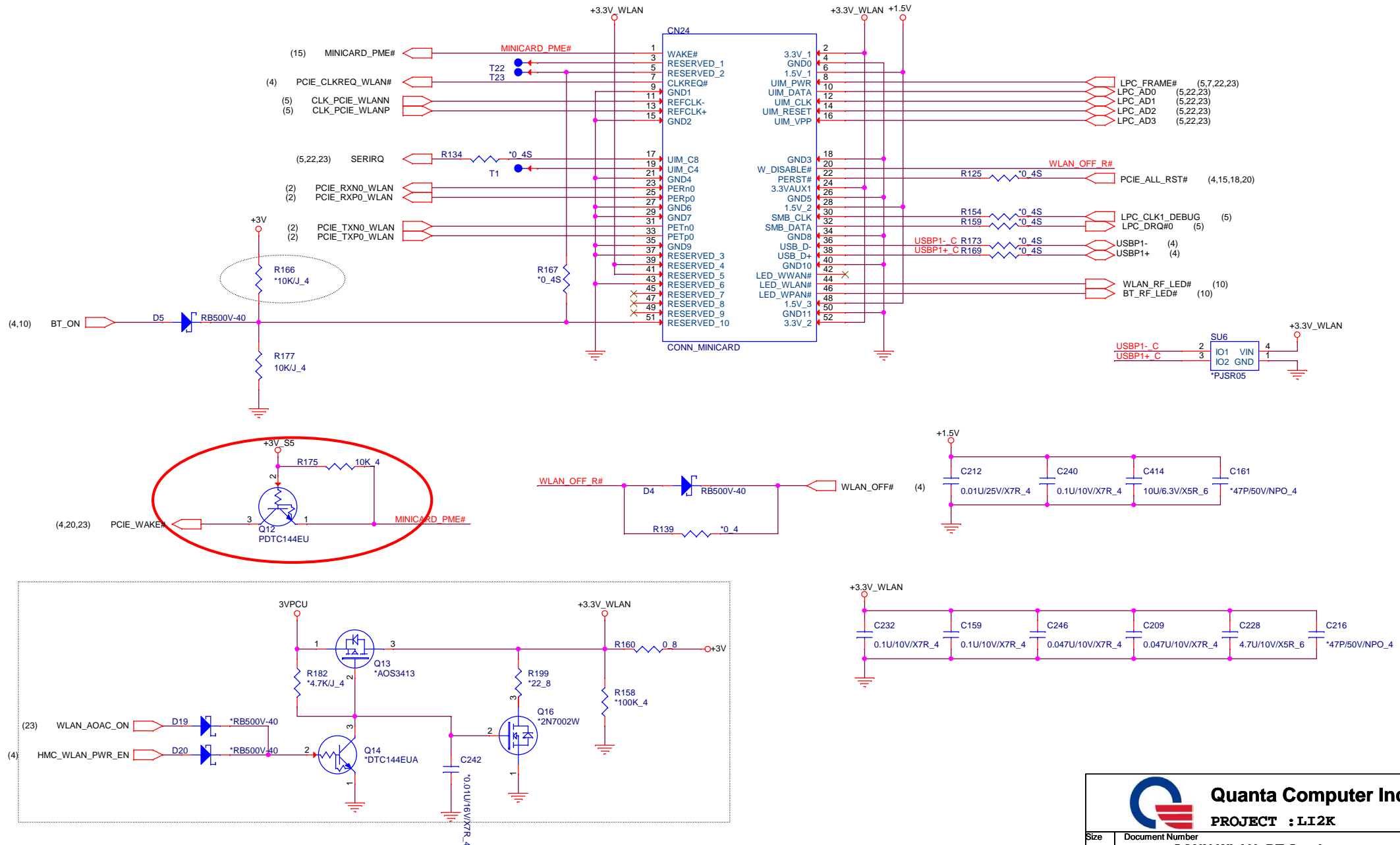
DC Current rating: 3 A (MAX)



Quanta Computer Inc.

PROJECT : LI2K

Size	Document Number	Rev
	CONN SATA(HDD or SSD)	3A
Date:	Wednesday, March 13, 2013	Sheet 12 of 35

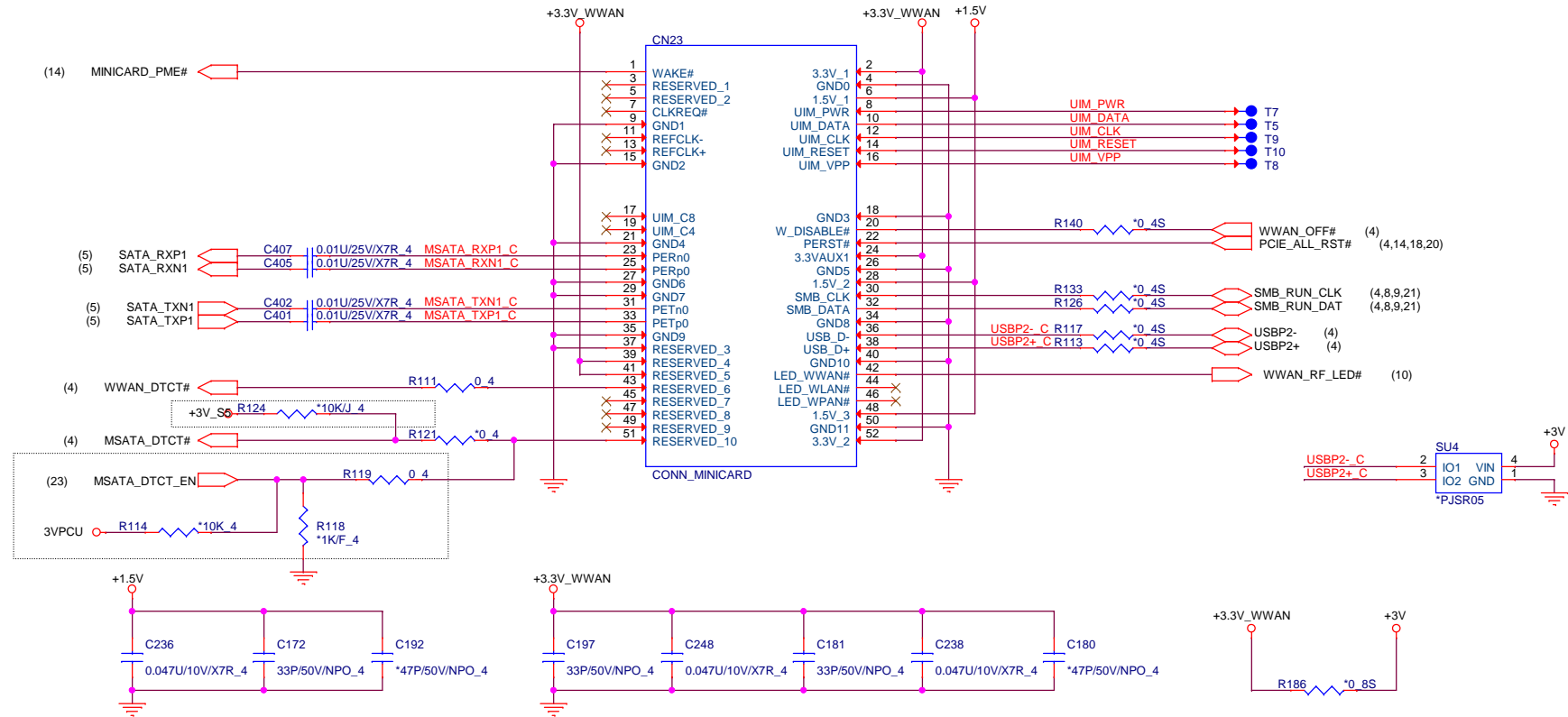


Quanta Computer Inc.

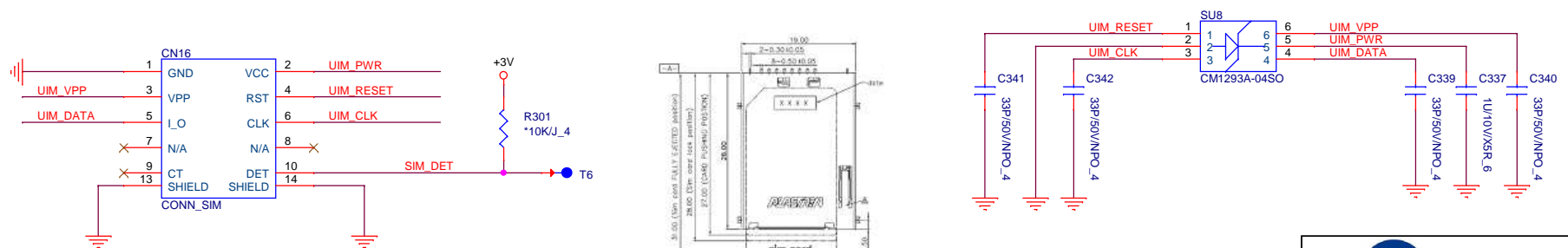
PROJECT : LI2K

Size	Document Number	Rev
	CONN WLAN+BT Combo	3A

Date: Wednesday, March 13, 2013 Sheet 14 of 35

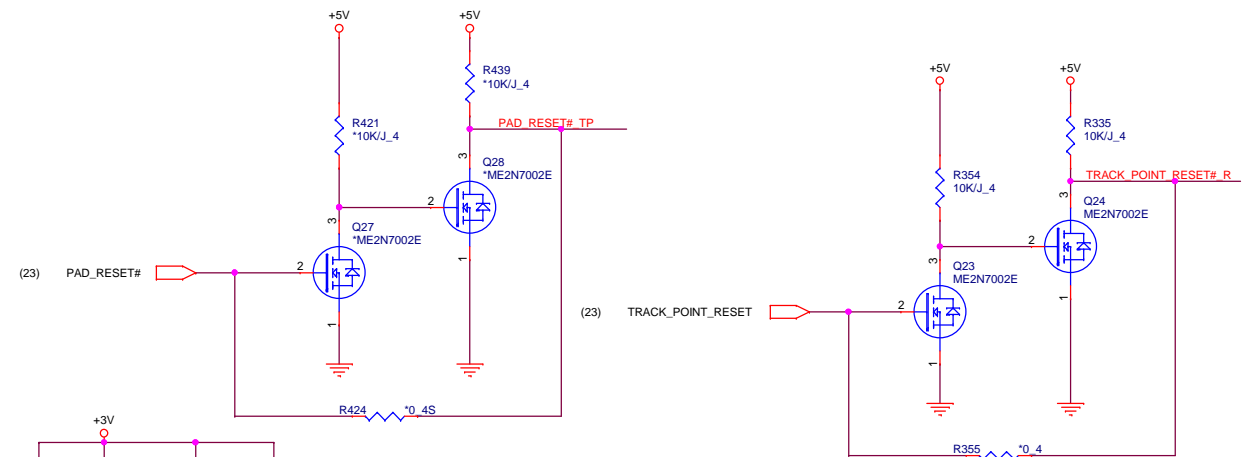
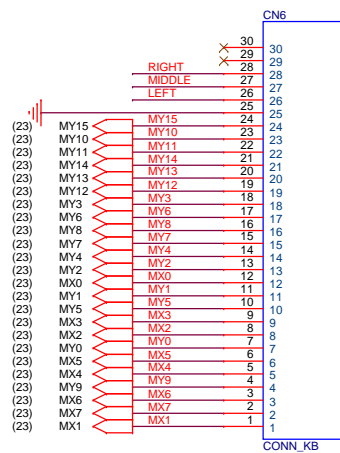


SIM Card CONN

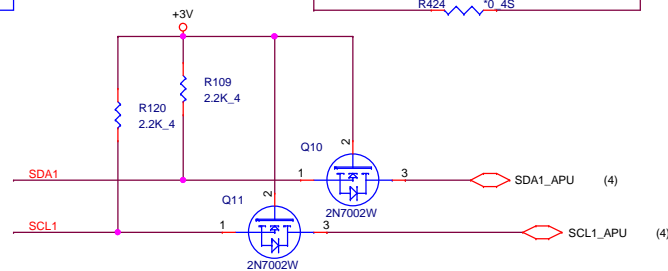


Layout Note: UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible

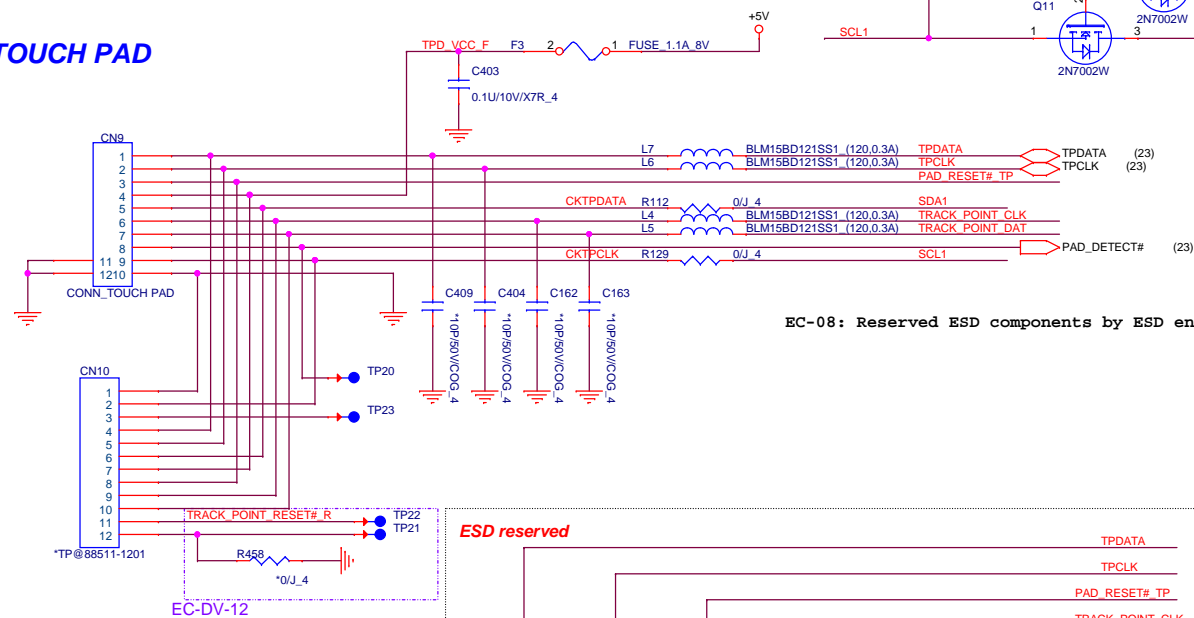
16



TOUCH PAD

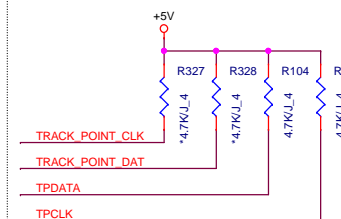
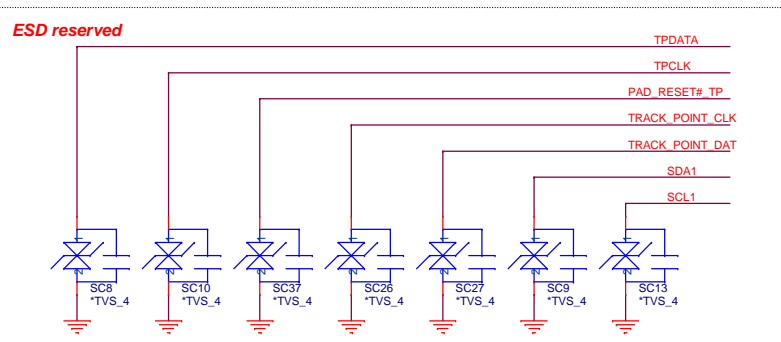
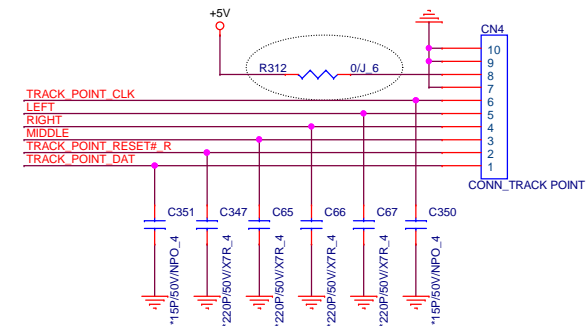


TRACK POINT



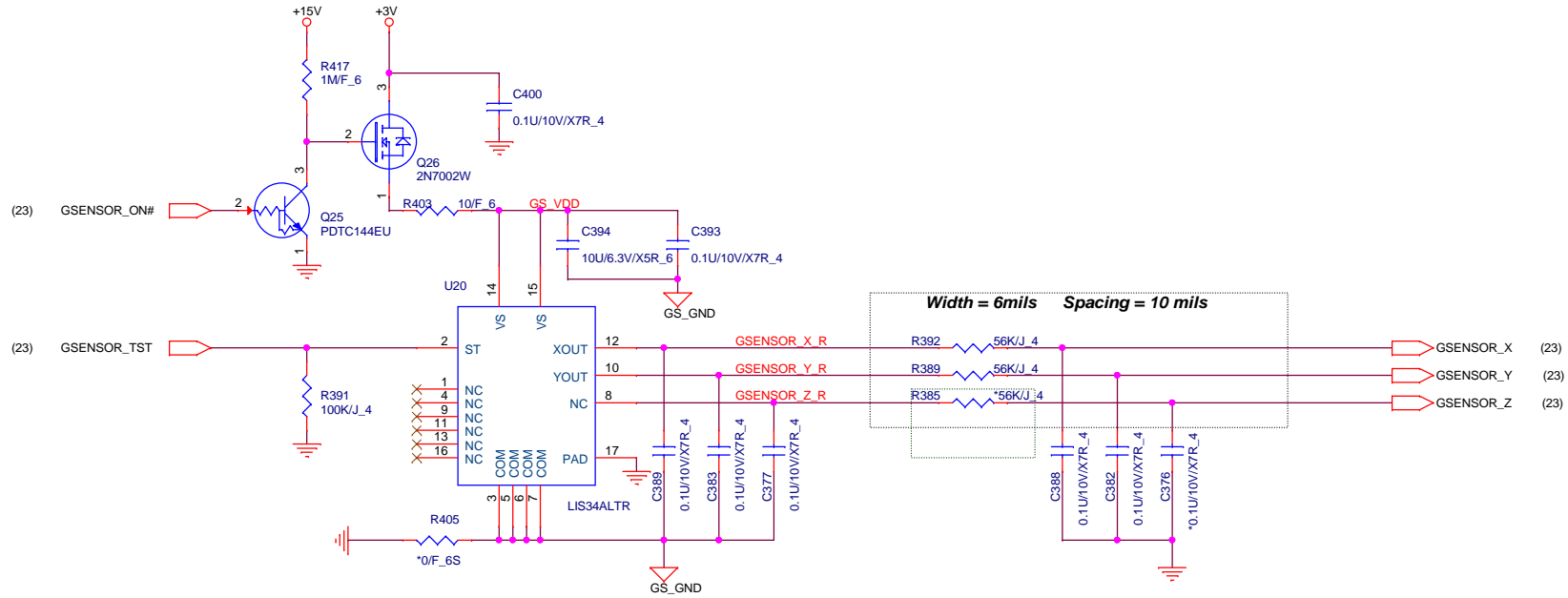
EC-08: Reserved ESD components by ESD engineer's suggestions

EC-C2-01: Reverse TRACK POINT Fuse.



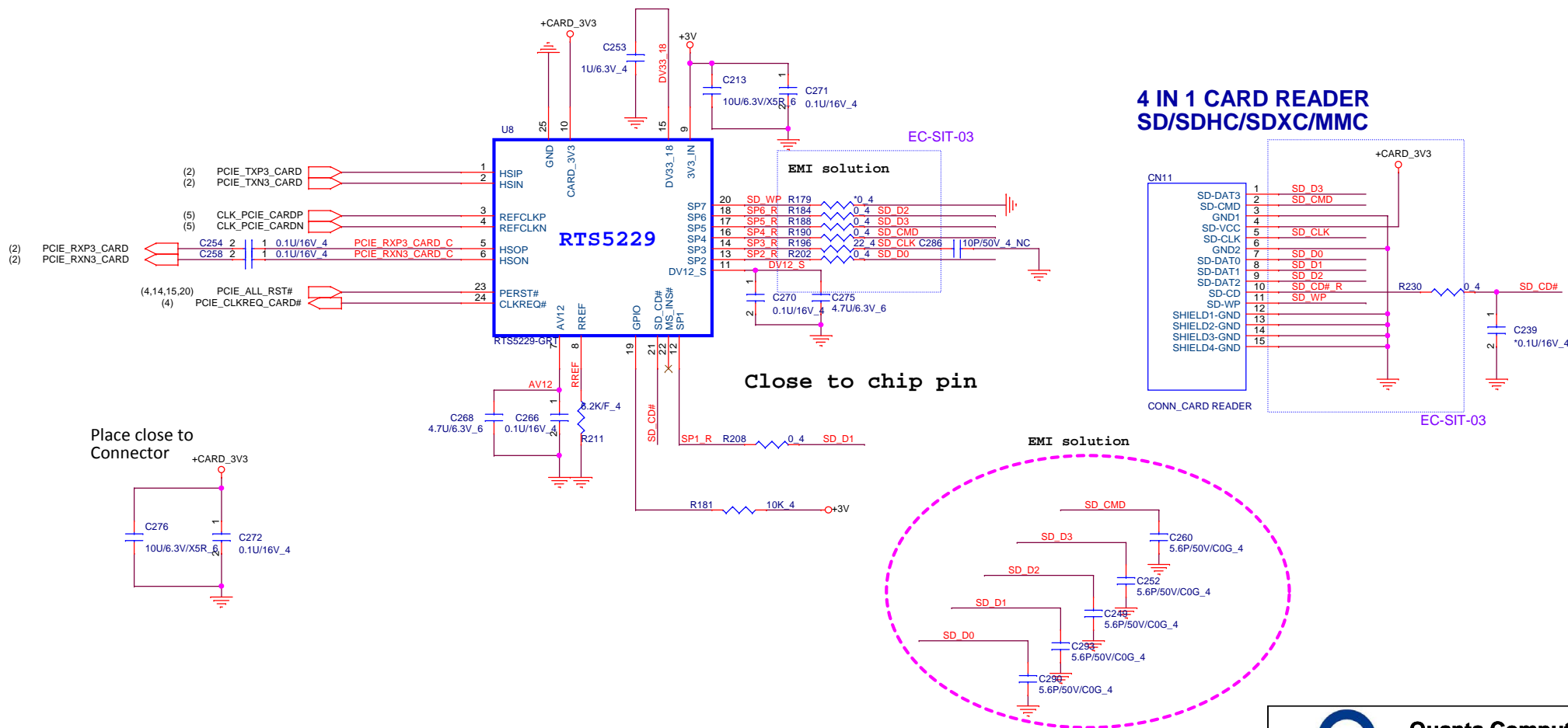
EC-B-10: Reverse SMBus CLICKPAD SCH.

G-SENSOR (2-Axial)



Cardreader (RTS5229) Support SD/ MMC

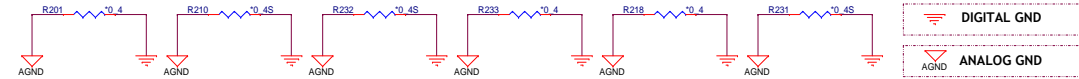
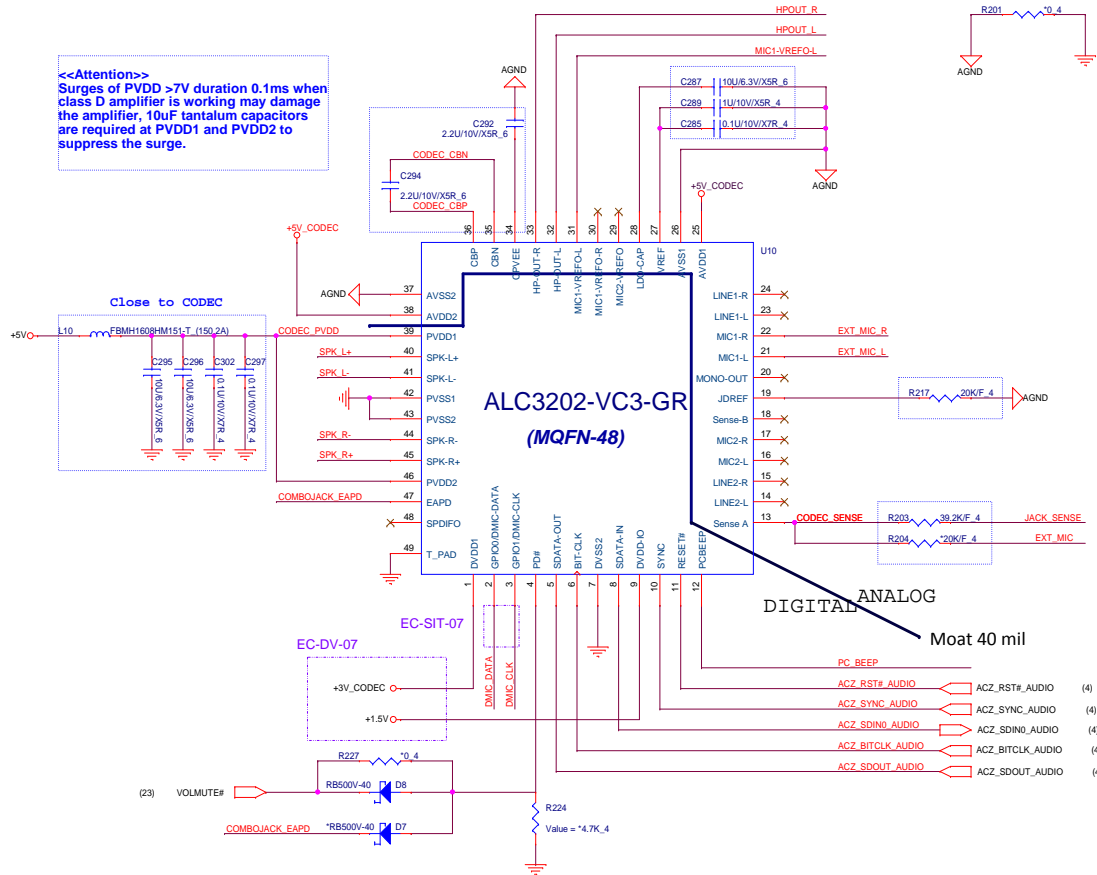
18



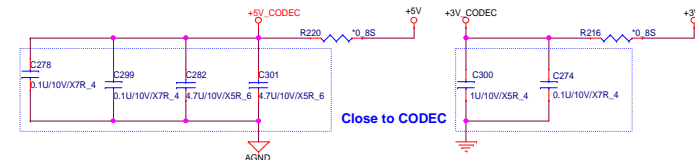
AUDIO CODEC: ALC3202-VC3-GR

EMI Reserve

Please see Design Guide for audio grounding

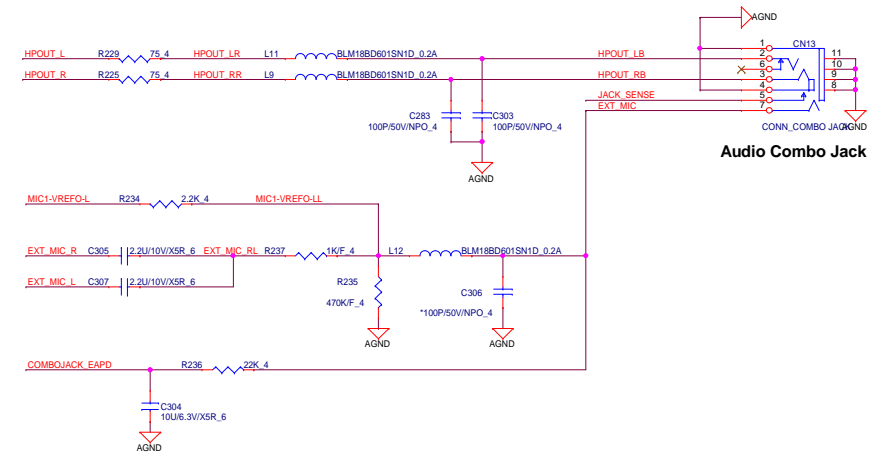


POWER

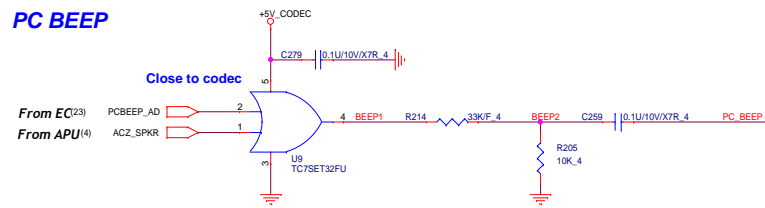


External MIC/Headphone Combo

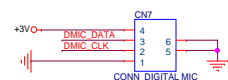
Important for Jack detect behavior: The Pin 4 & Pin 5 of COMBO-JACK must use Normal-Open type.



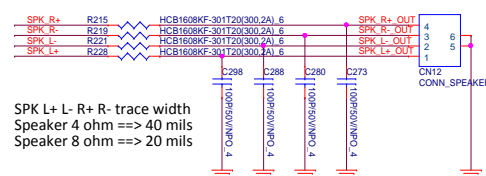
PC BEEP



INT Digital MIC

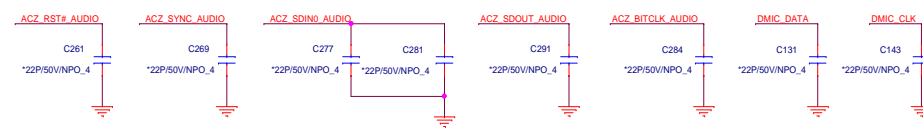


INT Speaker



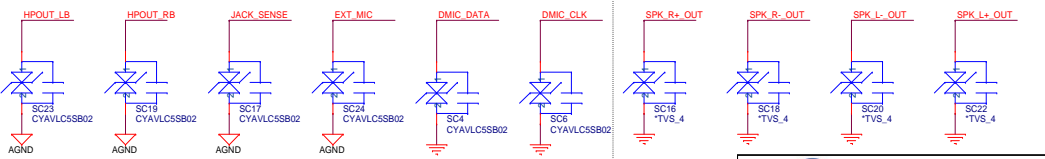
EMI Reserve

Place there EMI components next to codec; For EMI issue, please also refer our ALC269 Layout guide document



ESD Reserve

Reserved ESD components by ESD engineer's suggestions



20

The schematic shows a MOSFET-based driver circuit for a LANON signal. The input signal LAN_ON is connected to the gate of an AO4802A MOSFET through a 3VPCU voltage source. The MOSFET's drain is connected to a series combination of a resistor R172 (0J_8) and a capacitor C247 (C237), which is then connected to the LANVCC supply. A feedback path labeled LANVCC_R connects the output node back to the MOSFET's gate. The MOSFET's source is connected to ground through a network consisting of a 100nF capacitor (XSR_6) in parallel with a 0.1uF capacitor (WXR_4).

Place CAP. close to LAN IC pin 36

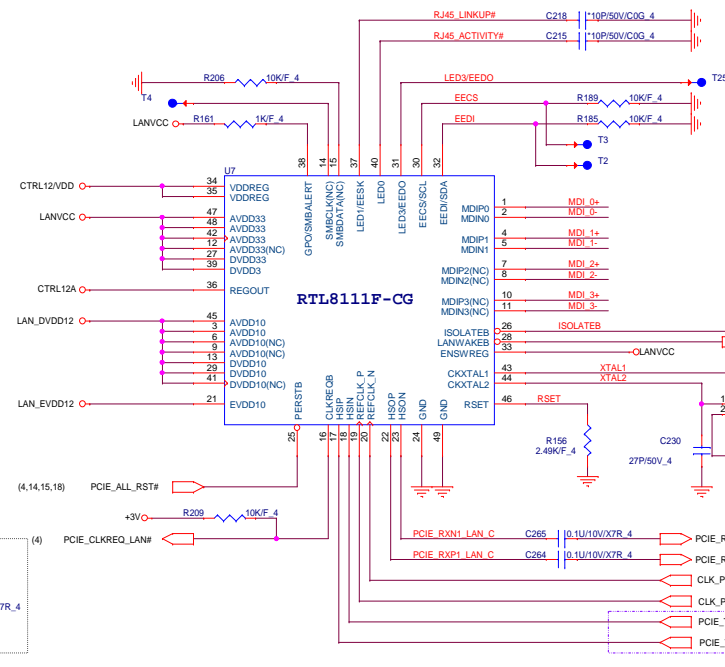
Place CAP. close to LAN IC pin 12, 27, 39, 42, 47, 48

Transformer

Layout: All termination signal should have 20 mil trace

Reserve for Surge and cable ESD

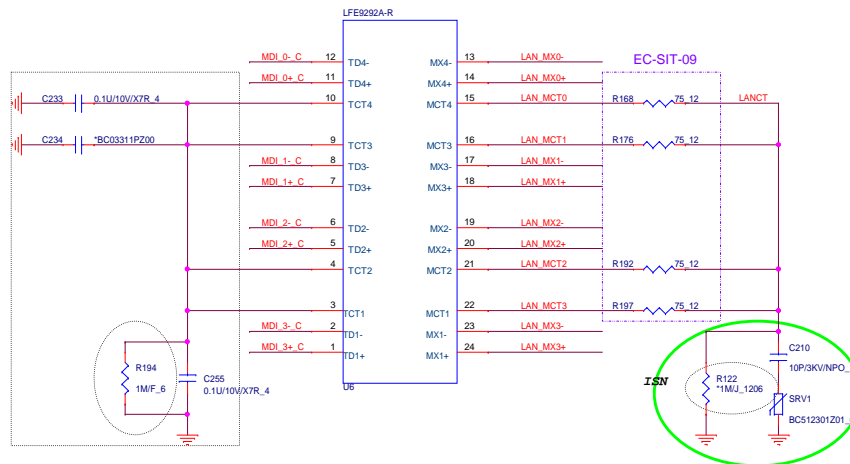
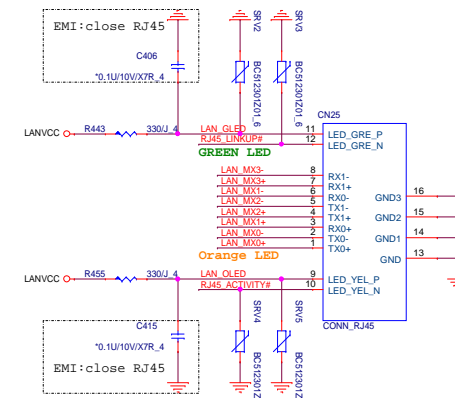
ESD request



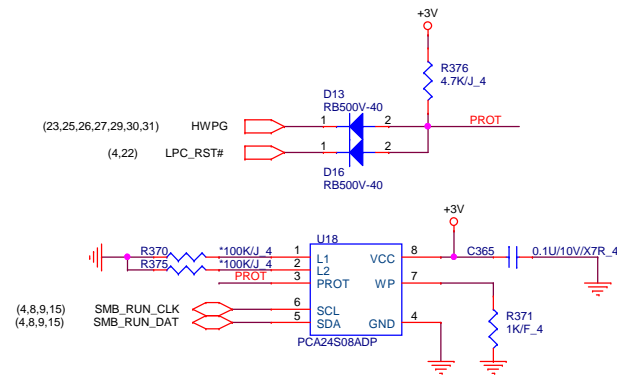
Isolate Pin: Active low.
Used to isolate the RTL811F from the PCI express bus. The RTL811F will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

EC-DV-06

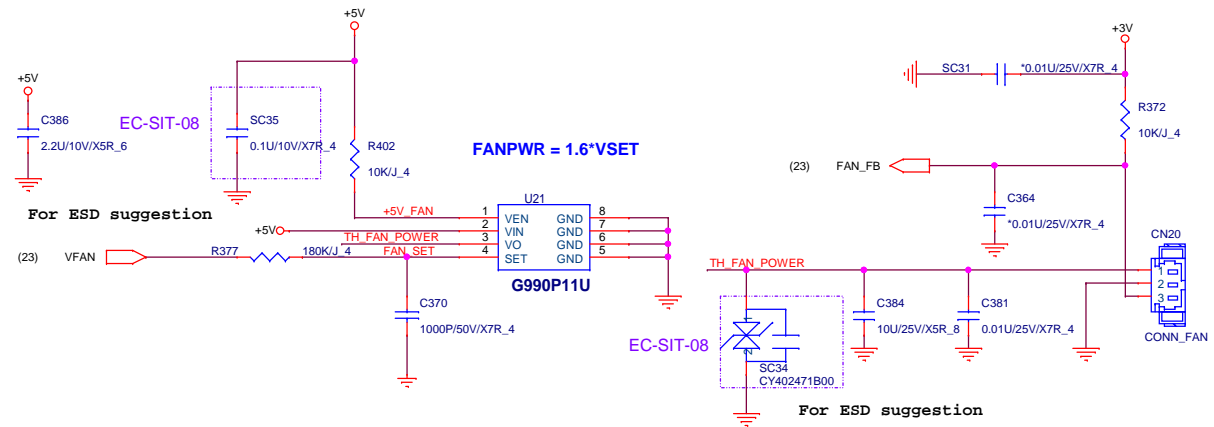
RJ45 Connector



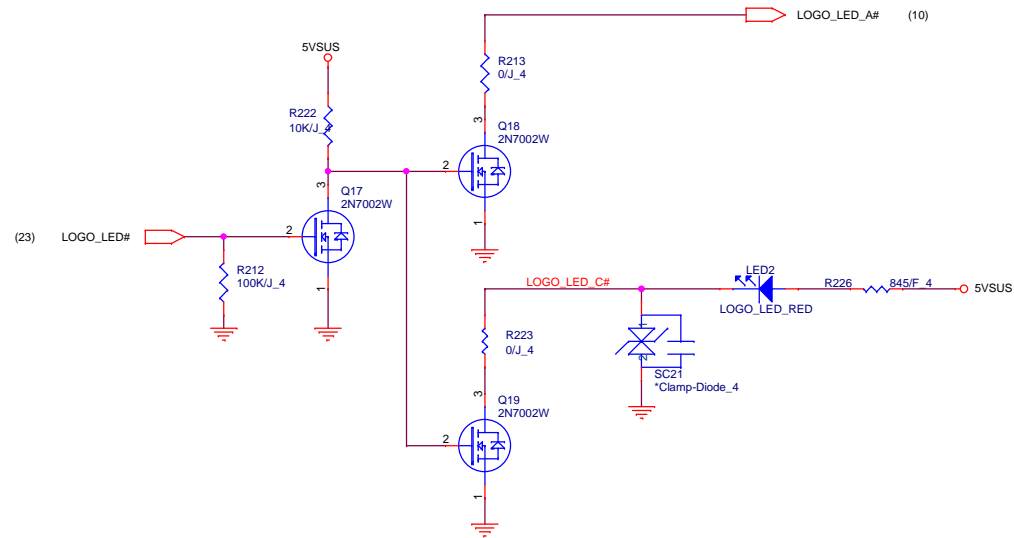
RFID



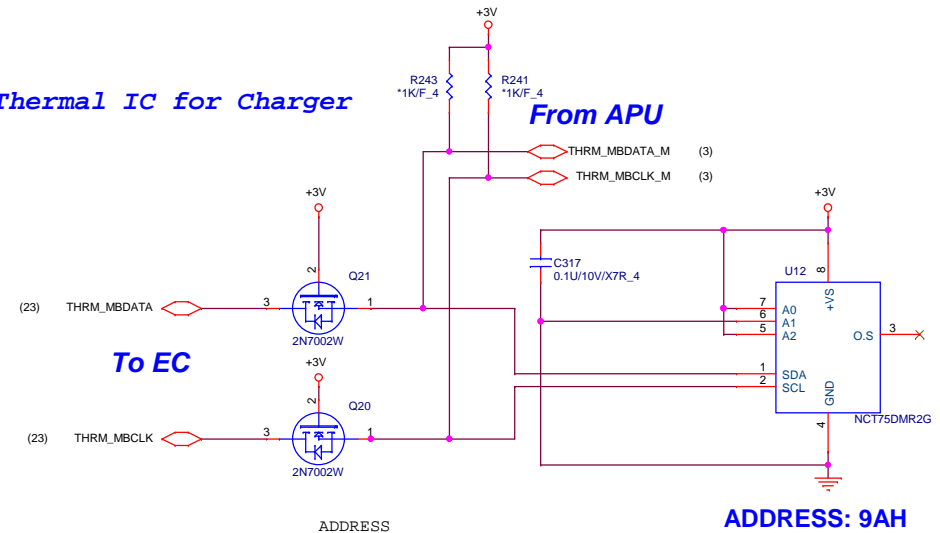
FAN IC & CONN



LED Driver

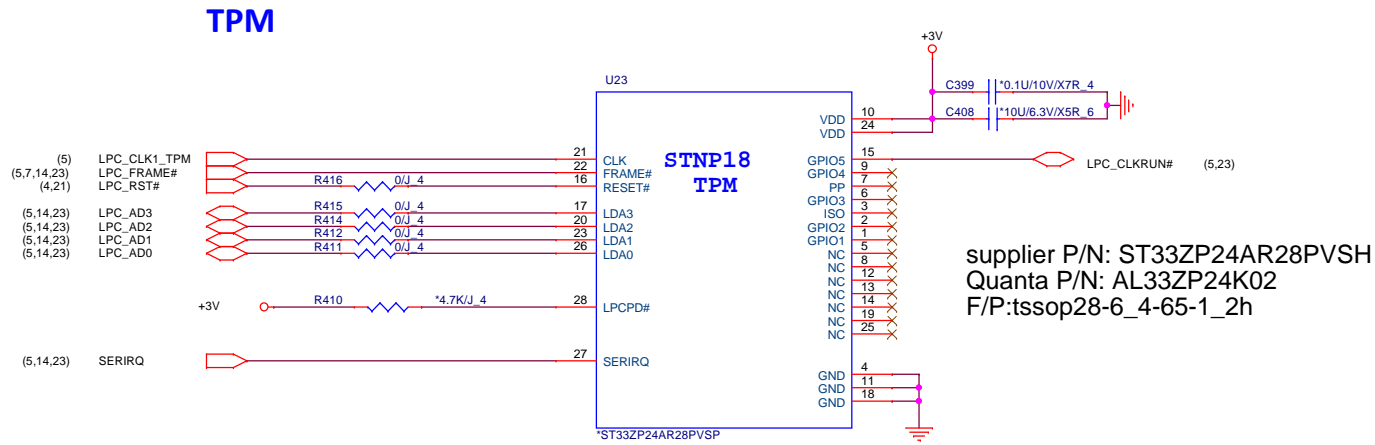


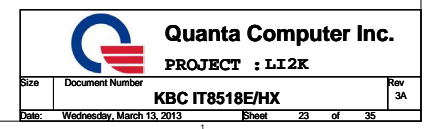
Thermal IC for Charger

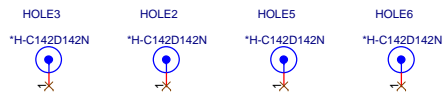
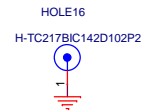
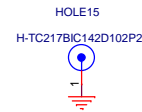
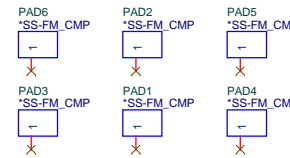
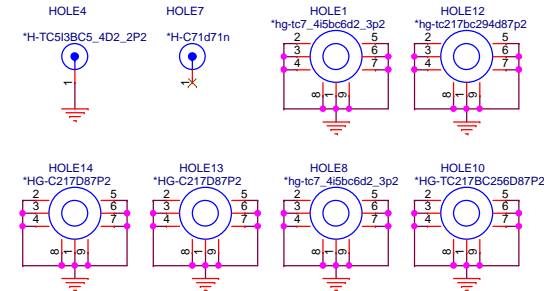
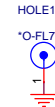
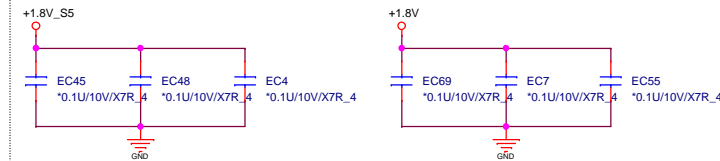
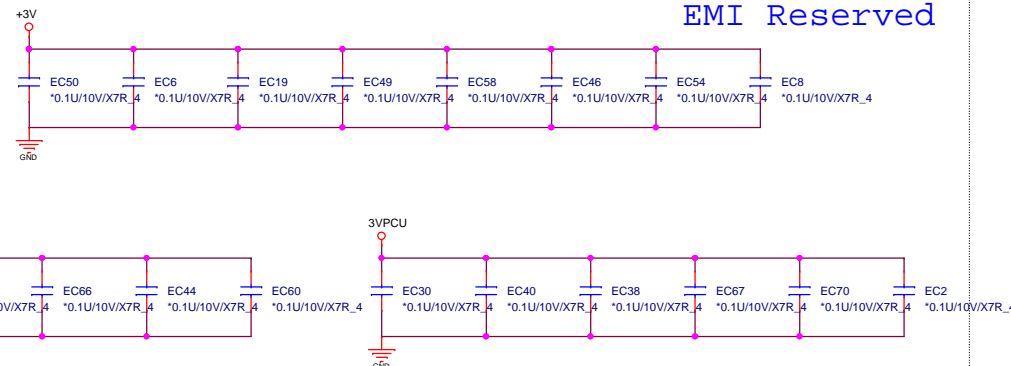
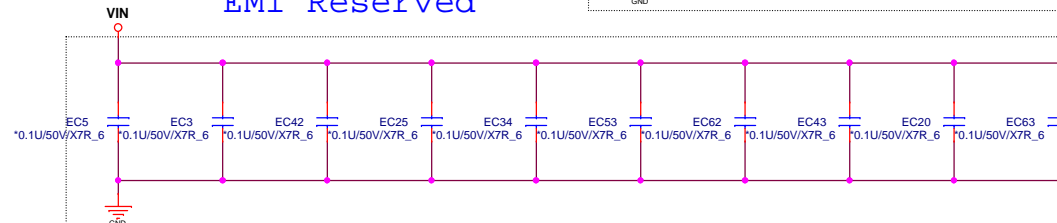
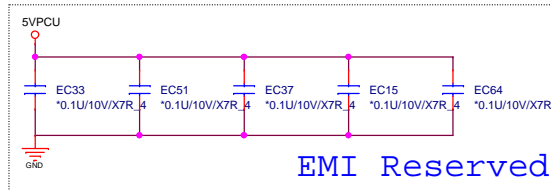
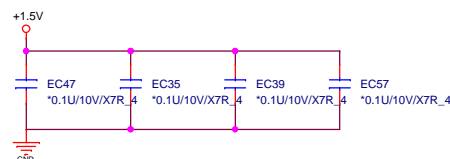


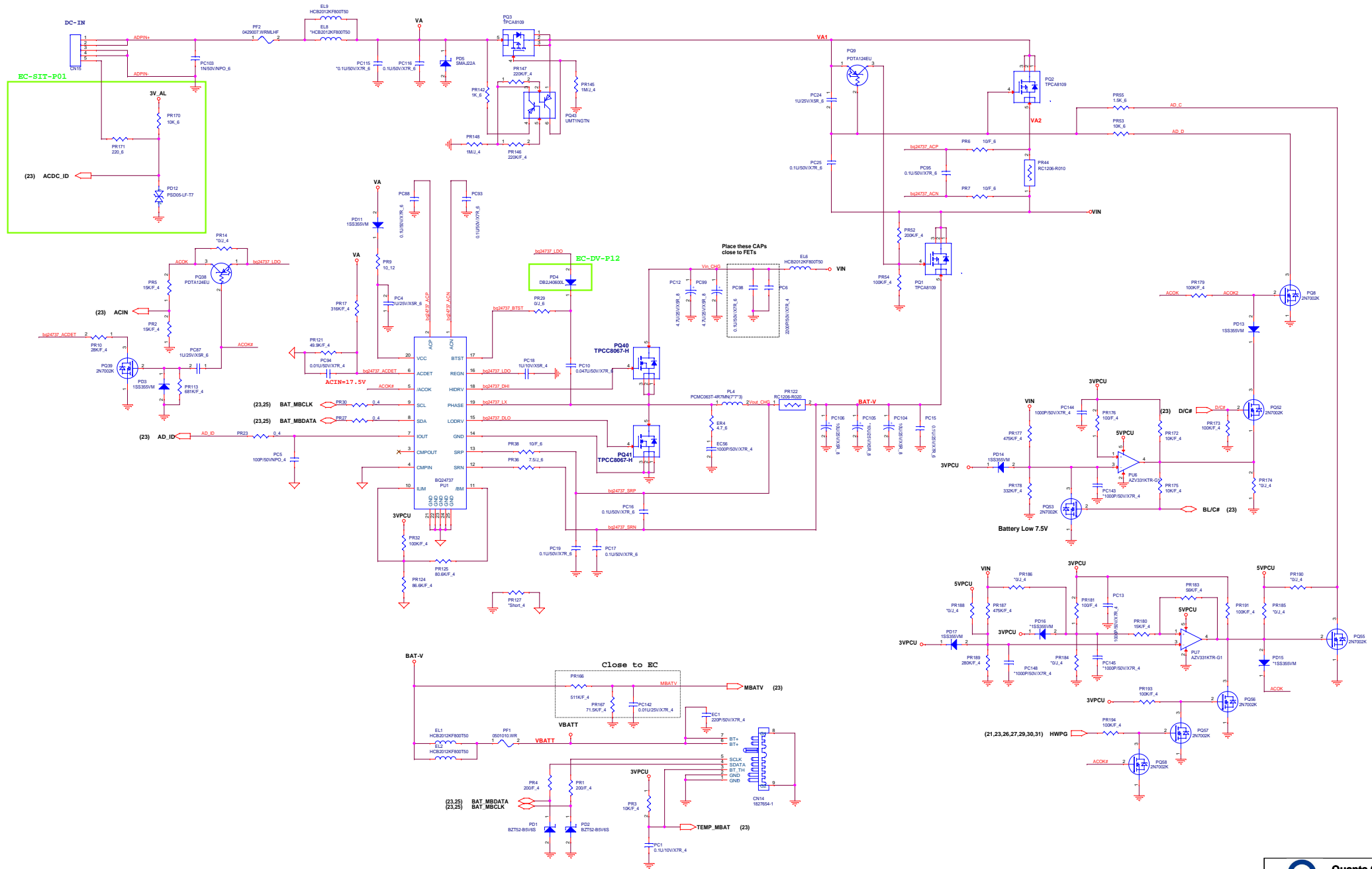
ADDRESS

1	0	0	1	A2	A1	A0	0
MSB				LSB			

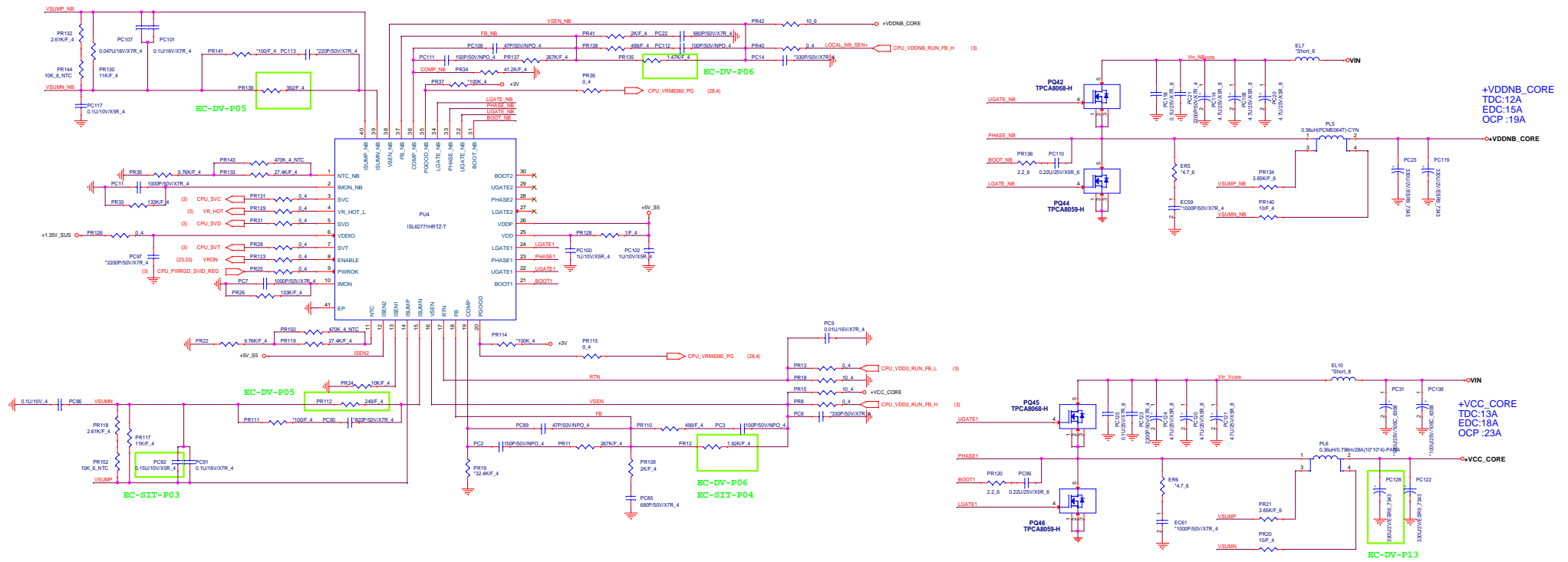




Hole For CPU support**MiniCard WWAN****MiniCard WLAN****Optics Point****Boundary Hole****CRT PAD****Keyboard****EMI Reserved****EMI Reserved****EMI Reserved****EMI Reserved****EMI Reserved**

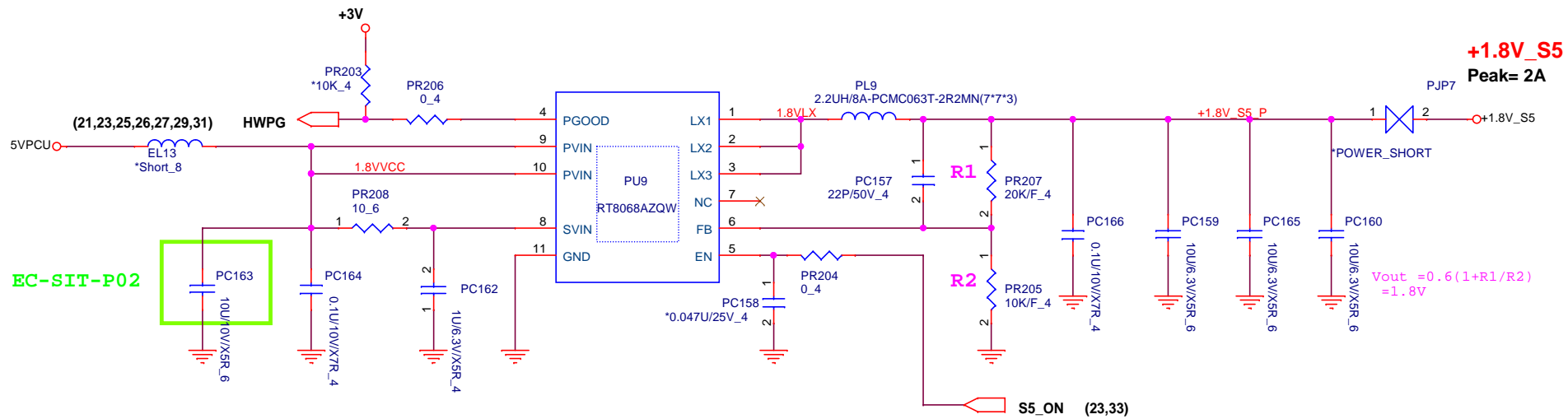


VCC_CORE/VDDNB_CORE (ISL62771HRTZ-T)



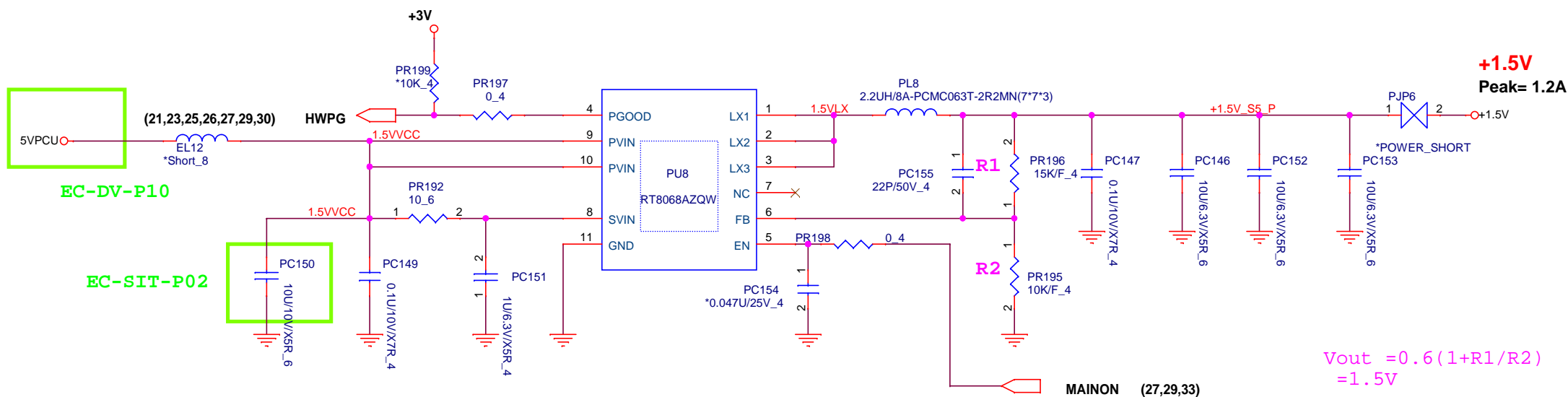
Freq. 290KHz
Peak = 7.1A
O.C.P.= 9.2A

Size	Document Number	Rev
	0.95V_S5(TPS51211)	1A
Date:	Wednesday, March 13, 2013	Sheet 29 of 34



Quanta Computer Inc.
PROJECT : LI2K

Size	Document Number	Rev
	+1.8V_S5 (RT8068)	3A
Date:	Tuesday, March 26, 2013	Sheet 30 of 34



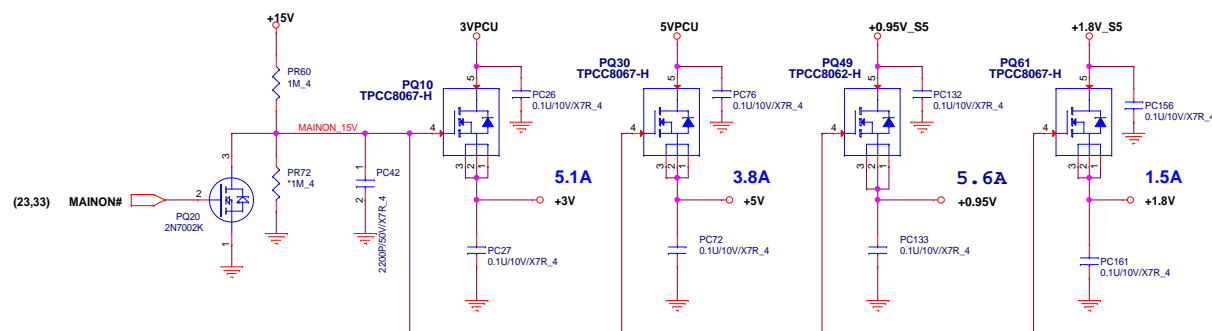
Quanta Computer Inc.

PROJECT : LI2K

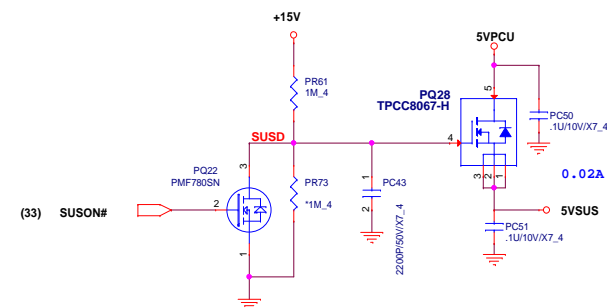
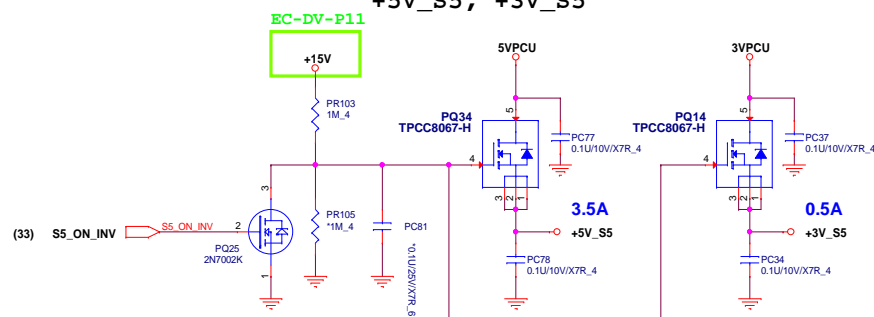
Size	Document Number	Rev
	+1.5V (RT8068)	3A

Date: Tuesday, March 26, 2013 Sheet 31 of 34

+3V, +5V, +0.95V, +1.8V, +1.5V



+5V_S5, +3V_S5



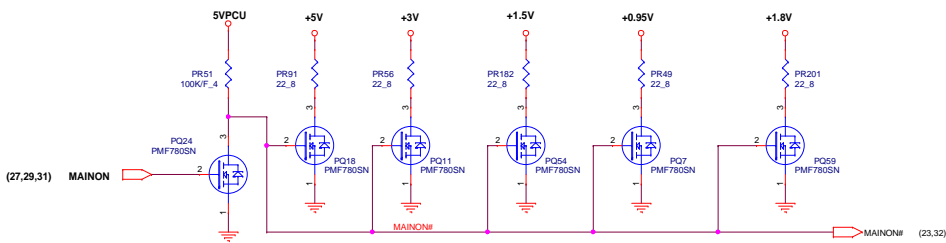
Quanta Computer Inc.

PROJECT : LI2K

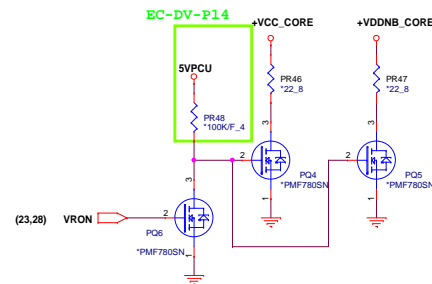
Size	Document Number	Rev
		1A
Load Switch		
Date:	Wednesday, March 13, 2013	Sheet 32 of 34

DISCHARGE

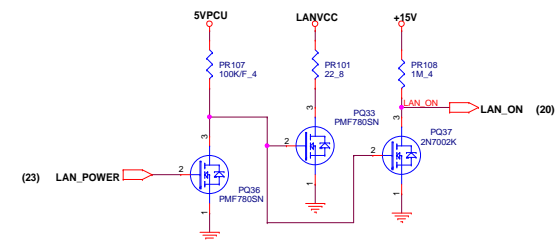
+3V, +5V, +1.5V, +0.95V, +1.8V



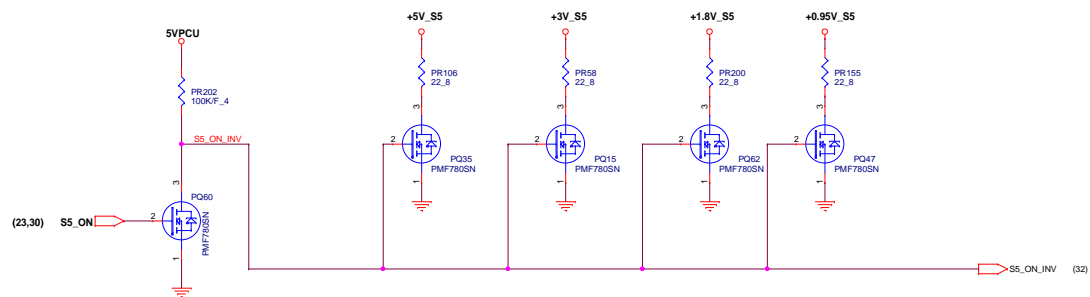
+VCC_CORE, +VDDNB_CORE



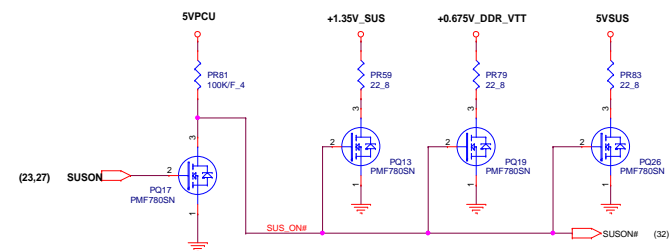
LANVCC



+1.5V_S5, +5V_S5, +3V_S5, +1.8V_S5, +0.95V_S5, +1.2V_S5

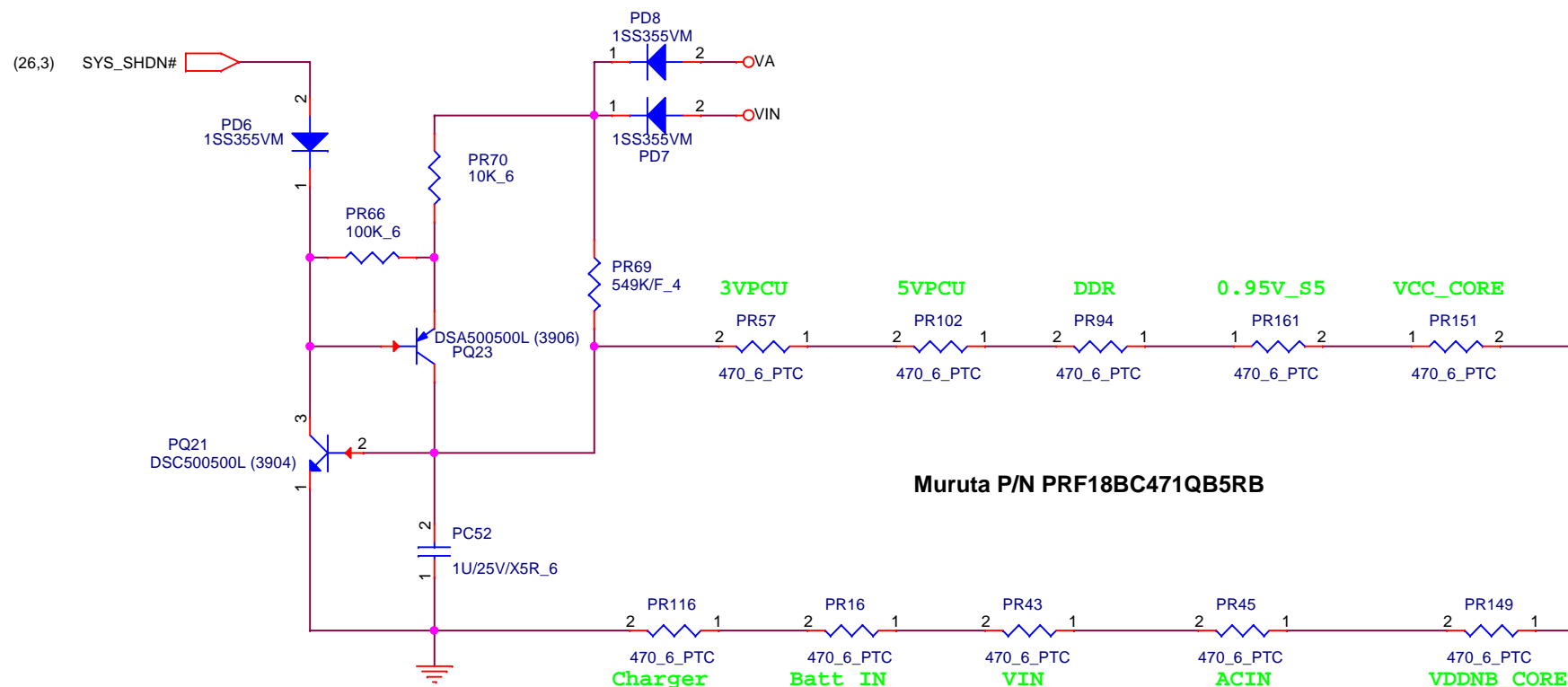


5VSUS, +1.35V_SUS, +0.675V_DDR_VTT



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LI2K Schematic EC Tracking Record A to B version

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EC #	Page	Description	Part Affected
EC-DV-01	6	Correct the footprint 0402 to 0603	C20,C50
EC-DV-02	23	Correct the Netname mainon# to mainon	
EC-DV-03	5	Change symbol pin number(Pin1 and Pin2)	U17
EC-DV-04	5	Change 32.768K XTAL Y2 to small one.	Y2,C324,C325
EC-DV-05	11	R447 stuff and connect the SMB data to fix HDMI no output.	R447
EC-DV-06	20	Swap the P/N net to correct.	
EC-DV-07	19	Change audio VDDIO to +1.5V for Kabini platform only	
EC-DV-08	2	R362 stuff by AMD confirmation	R362
EC-DV-09	23	Reserved the path 3VPCU/+3V for EC pin 11 to prevent currnet leakage	R456,R457
EC-DV-10	11	R146 change the value from 464 to 499	R146
EC-DV-11	13	Increase the USB FFC power pin	
EC-DV-12	16	Modify CN10 Pin 11,Pin 12	
EC-DV-13	11	Un-stuff to Stuff for EMI solution in HDMI	R420,R425,R430,R438
EC-DV-14	10,13	Stuff for EMI Common choke in USB	CML1,CML2,CML3,CML4,R19,R23,,R86,R87,R101,R102,R131,R132
EC-DV-15	4,23	Un-stuff to Stuff for EMI solution	C328,C372
EC-DV-16	24	Un-stuff to Stuff for EMI solution	SC5,SC7,SC11,SC15
EC-DV-17	11	Chagne the value for EMI suggestion	L1,L2,L3,C2,C5,C8,C11,C12,C15
EC-DV-18			
EC-DV-19			
EC-DV-20			
EC-DV-21			
EC-DV-22			
EC-DV-23			
EC-DV-24			
EC-DV-25			
EC-DV-26			
EC-DV-27			
EC-DV-28			
EC-DV-29			
EC-DV-30			

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Power EC RECORD B to C		
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